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EXAMINER	
CHOI, EUNSOOK	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,164	SCHULTZ, ROBERT J.	
	Examiner	Art Unit	
	Eunsook Choi	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 12, 13, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kaganoi et al (US PGPUB 20030012198).

Regarding claim 12, Kaganoi teaches a packet processing unit in Fig. 3. In Abstract, a packet receiving circuit 11 splits the packet received from a transmission channel 1 into a fixed length of cells and outputs the cells, a search key extracting circuit 12 extracts a predetermined search key from the above-mentioned cells (at least one first stage processing element), a CAM 13 performs retrieval based on the above-mentioned search key (a first stage memory unit that is searched in response to search information from the first stage processing element) and outputs a memory address corresponding to the search key, a matching entry address receiving and associative data address transmitting circuit 14 calculates the memory address of an associative data memory (the second stage processing element to perform search-independent

processing related to a packet in parallel with a search of the first stage memory unit, where the search is related to the same packet).

Regarding claim 13, Kaganoi teaches [0038] and [0039] the CAM 13 performs retrieving process based on the search key input from the search key extracting circuit 12 and outputs a memory address of the CAM 13 to the matching entry address receiving and associative data address transmitting circuit 14 (a direct communications link between the first stage memory unit and the second stage processing element configured to provide search results directly to the second stage processing element from the first stage memory unit).

Regarding claim 17, Kaganoi teaches the first stage memory unit comprises content addressable memory in Fig. 3.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 6, 7, 8, 9, 11, 14, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaganoi et al. (US PGPUB 20030012198) in view of Kanakubo (US Patent 7,158,519).

Regarding claim 1, Kaganoi teaches a packet processing unit in Fig. 3. In Abstract, a packet receiving circuit 11 splits the packet received from a transmission channel 1 into a fixed length of cells and outputs the cells, a search key extracting circuit 12 extracts a predetermined search key from the above-mentioned cells (a first search related to a packet using first search information), a CAM 13 performs retrieval based on the above-mentioned search key (a first stage memory unit that is searched in response to search information from the first stage processing element) and outputs a memory address corresponding to the search key, a matching entry address receiving and associative data address transmitting circuit 14 calculates the memory address of an associative data memory (performing, in parallel with the first search, search-independent processing on information related to the packet).

However, Kaganoi does not expressly teach producing second search information. Kanakubo teaches in Fig. 1, Fig. 11 and Col. 8 Lines 12-22 a search of the account entries, the congestion avoiding entries, the QoS entries, and default entries. If setting of the account entries is not performed in S11, and the process moves on to the second search. Kanakubo further teaches in Col. 2 Lines 1-9 the current hardware functionally performs two searches, a search for a QoS flow entry and a search for a routing entry, in the search process for the CAM 12, and the registration of the search keys is performed by software. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce second search information in order to provide Quality of Service assurance in IP packet transfer (Col.1 Lines 16-24 Kanakubo).

Regarding claim 6, Kaganoi teaches in Fig. 3 and Abstract a search key extracting circuit 12 extracts a predetermined search key from the packet (processing information related to a packet using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements), a CAM 13 performs retrieval based on the above-mentioned search key (the search of the first stage memory unit) and outputs a memory address corresponding to the search key, a matching entry address receiving and associative data address transmitting circuit 14 calculates the memory address of an associative data memory (performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet using a second stage processing element). However, Kaganoi does not expressly teach producing a second search key, searching a second stage memory unit using the second search key. Kanakubo teaches in Fig. 1, Fig. 11 and Col. 8 Lines 12-22 a search of the account entries, the congestion avoiding entries, the QoS entries, and default entries. If setting of the account entries is not performed in S11, and the process moves on to the second search. Kanakubo further teaches in Col. 2 Lines 1-9 the current hardware functionally performs two searches, a search for a QoS flow entry and a search for a routing entry, in the search process for the CAM 12, and the registration of the search keys is performed by software. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a second search key and searching a

second stage memory unit using the second search key in order to provide Quality of Service assurance in IP packet transfer (Col.1 Lines 16-24 Kanakubo).

Regarding claim 2, Kaganoi and Kanakubo teach the limitations for claim 1. However, Kaganoi does not expressly a second search using the second search information. Kanakubo teaches in Fig. 1, Fig. 11 and Col. 8 Lines 12-22 a search of the account entries, the congestion avoiding entries, the QoS entries, and default entries. If setting of the account entries is not performed in S11, and the process moves on to the second search. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a second search key and searching a second stage memory unit using the second search key in order to provide Quality of Service assurance in IP packet transfer (Col.1 Lines 16-24 Kanakubo).

Regarding claim 3, Kaganoi and Kanakubo teach the limitations for claim 2. Kaganoi teaches in Fig. 3 associative data address transmitting circuit 14 waits for out from CAM13 (holding a processing state from the search-independent processing until the result from the first search is available).

Regarding claim 7, Kaganoi teaches [0039] the matching entry address receiving and associative data address transmitting circuit 14 (the search-independent processing) in Fig. 3 receives the above-mentioned memory address from the CAM 13 and calculates a memory address of the associative data memory (holding a processing

state from the search-independent processing until the result from the search of the first stage memory unit is received at the second stage processing element).

Regarding claims 8 and 9, Kaganoi and Kanakubo teach the limitations for claims 6 and 7. Kaganoi teaches [0039] the matching entry address receiving and associative data address transmitting circuit 14 (the second stage processing element) in Fig. 3 receives the above-mentioned memory address from the CAM 13 and calculates a memory address of the associative data memory (providing the result from the search of the first stage memory unit directly to the second stage processing element from the first stage memory unit).

Regarding claim 11, Kaganoi teaches the pipeline process in Fig. 3 with a white wide arrow between the search key extracting circuit 12 and the matching entry address receiving and associative data address transmitting circuit 14 (forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced). [0061] the packet transmitting circuit 17 for generating packets by merging the cells from the search result (associative data) receiving circuit 16 and outputting the packet to a transmission channel 2. The packet processing unit is characterized in that the packet receiving circuit 11, the search key extracting circuit 12, the CAM 13, the associative data memory 15, the matching entry address receiving and associative data address transmitting circuit 14, the search result

(associative data) receiving circuit 16, and the packet transmitting circuit 17 perform the pipeline process.

Regarding claim 14, Kaganoi teaches the limitations for claim 12. However, Kaganoi does not expressly teach producing a second search key. Kanakubo teaches in Fig. 1, Fig. 11 and Col. 8 Lines 12-22 a search of the account entries, the congestion avoiding entries, the QoS entries, and default entries. If setting of the account entries is not performed in S11, and the process moves on to the second search. Kanakubo further teaches in Col. 2 Lines 1-9 the current hardware functionally performs two searches, a search for a QoS flow entry and a search for a routing entry, in the search process for the CAM 12, and the registration of the search keys is performed by software. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a second search key and searching a second stage memory unit using the second search key in order to provide Quality of Service assurance in IP packet transfer (Col.1 Lines 16-24 Kanakubo).

Regarding claim 15, Kaganoi and Kanakubo teaches the limitations for claim 14. However, Kaganoi does not expressly teach the search key is used to search the second stage memory unit. Kanakubo teaches in Col. 2 Lines 1-9 the current hardware functionally performs two searches, a search for a QoS flow entry and a search for a routing entry, in the search process for the CAM 12, and the registration of the search keys is performed by software. It would be obvious to one having ordinary skill in the art

at the time of the invention was made to produce a second search key and searching a second stage memory unit using the second search key in order to provide Quality of Service assurance in IP packet transfer(Col.1 Lines 16-24 Kanakubo).

Regarding claim 16, Kaganoi and Kanakubo teaches the limitations for claim 15. However, Kaganoi does not expressly teach the third stage processing element to perform search-independent processing related to the packet in parallel with the search of the second stage memory unit. Kanakubo teaches in Fig. 1 (refer to item numbers 22, 23, 24, and 25), Fig. 11 and Col. 8 Lines 12-22 a search of the account entries, the congestion avoiding entries, the QoS entries, and default entries. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a second search key and searching a second stage memory unit using the second search key in order to provide Quality of Service assurance in IP packet transfer(Col.1 Lines 16-24 Kanakubo).

5. Claims 4, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaganoi (US PGPUB 20030012198) modified by Kanakubo (US Patent 7,158,519) as applied to claims 1 and 6 above, and further in view of Khanna (US Patent 7219187).

Regarding claim 4, Kaganoi and Kanakubo teach the llimitations for claim 1. However, Kaganoi and Kanakubo do not teach producing a comparand and a mask as the second search information. Khanna teaches in Col. 2 Lines 10-19 the CAM device

can be instructed by the processor to compare a search key, also referred to as a comparand (e.g., generated from packet header data), with data stored in its associative memory array. Khanna further teaches in Col. 9 Lines 31-62 global mask select circuit 607 selects the corresponding global mask ID (GMID 622) from search parameter table 525 in response to the activated GMSEL signal. The selected GMID is used to select a corresponding global mask GM(1) GM(z) from the global mask register 606 that globally masks the comparand data during a compare operation. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

Regarding claim 5, Kaganoi and Kanakubo teach the llimitations for claim 4. However, Kaganoi and Kanakubo do not teach the second search includes searching a content addressable memory (CAM) using the comparand and the mask. Khanna teaches in Fig. 6 and Col. 9 Lines 31-62 Block select circuit 605 outputs block select signal BSEL 609 that enables comparand drivers 608 to drive the comparand data into CAM block array 602 to participate in a compare operation if a stored CAM table ID for the CAM array 602 matches one of the CAM table IDs provided from the search parameter table 525. the comparand data is globally masked by the selected global mask data by logically ANDing together the selected global mask data on a bit-for-bit basis with corresponding bits of the comparand data in the comparand drivers 608. It would be obvious to one having ordinary skill in the art at the time of the invention was

made to search a content addressable memory (CAM) using the comparand and the mask in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

Regarding claim 10, Kaganoi and Kanakubo teach the llimitations for claim 6. However, Kaganoi and Kanakubo do not teach search keys include a comparand and a mask. Khanna teaches in Fig. 6 and Col. 9 Lines 31-62 Block select circuit 605 outputs block select signal BSEL 609 that enables comparand drivers 608 to drive the comparand data into CAM block array 602 to participate in a compare operation if a stored CAM table ID for the CAM array 602 matches one of the CAM table IDs provided from the search parameter table 525. the comparand data is globally masked by the selected global mask data by logically ANDing together the selected global mask data on a bit-for-bit basis with corresponding bits of the comparand data in the comparand drivers 608. It would be obvious to one having ordinary skill in the art at the time of the invention was made to include a comparand and a mask in search keys in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

6. Claims 18, 19, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaganoi (US PGPUB 20030012198) and in view of Khanna (US Patent 7219187).

Regarding claim 18, Kaganoi teaches a packet processing unit in Fig. 3. In Abstract, a packet receiving circuit 11 splits the packet received from a transmission channel 1 into a fixed length of cells and outputs the cells, a search key extracting circuit 12 extracts a predetermined search key from the above-mentioned cells (a first stage processing element), a CAM 13 performs retrieval based on the above-mentioned search key (a memory interface that is configured to provide search information to a first stage memory unit) and outputs a memory address corresponding to the search key, a matching entry address receiving and associative data address transmitting circuit 14 calculates the memory address of an associative data memory (a second stage processing element). However, Kaganoi does not expressly teach a plurality of first and second stage processing elements, a first stage memory unit from the plurality of first stage processing elements and to the plurality of second stage processing elements. Khanna teaches in Col. 4 Lines 39-50 a smaller IBUS can be utilized when compared with other CAM devices that provide both the search parameters explicitly over the IBUS. For example, use of the search parameter table can be particularly advantageous for CAM devices that can perform multiple concurrent compare operations because the number of input pins of the CAM device can be reduced to accommodate the selection code. Without the search parameter table, a user would need to provide all of the search parameters (e.g., CAM table IDs and global mask register IDs for all of the compare operations) directly on the IBUS or other bus such as a data bus. It would be obvious to on having ordinary skill in the art at the time of the invention was made to have a plurality of first and second stage processing elements, a first stage memory unit

from the plurality of first stage processing elements and to the plurality of second stage processing elements because it can be particularly advantageous for CAM devices that can perform multiple concurrent compare operations (in Col. 4 Lines 39-50 Khanna).

Regarding claim 19, Kaganoi and Khanna teach the limitations for claim 18. Kaganoi teaches the pipeline process in Fig. 3 with a big wide arrow between [0061] the search key extracting circuit 12 and the matching entry address receiving and associative data address transmitting circuit 14 (the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit, where the searches are related to the same packets).

Regarding claim 20, Kaganoi and Khanna teach the limitations for claim 18. Kaganoi teaches the pipeline process in Fig. 3 with a big wide arrow between [0061] the search key extracting circuit 12 and the matching entry address receiving and associative data address transmitting circuit 14 (the first stage processing elements forward information to respective second stage processing elements before results from respective searches of the first stage memory unit are received by the second stage processing elements).

Regarding claim 21, Kaganoi and Khanna teach the limitations for claim 18. However, Kaganoi does not expressly teach a first bus or a second bus to the memory

interface. Khanna teaches in Col. 4 Lines 39-50 a smaller IBUS can be utilized. It would be obvious to on having ordinary skill in the art at the time of the invention was made to have a plurality of first and second stage processing elements, a first stage memory unit from the plurality of first stage processing elements and to the plurality of second stage processing elements because it can be particularly advantageous for CAM devices that can perform multiple concurrent compare operations (in Col. 4 Lines 39-50 Khanna).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eunsook Choi whose telephone number is 571-270-1822. The examiner can normally be reached on Monday-Friday 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eunsook Choi
8/17/2007